

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on April 14, 2004, and the references cited therewith.

Claims 1, 7-9, 11, 17-19, 21, 23, 24, 26-29, 31-34, 36, and 37 are amended, and no claims are canceled or added; as a result, claims 1-38 are now pending in this application.

§112 Rejection of the Claims

Claims 1, 11, 21 and 31 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Each of claims 1, 11, 21, and 31 were rejected because language regarding a “FRIT kernel” and “kernel test vectors” was considered indefinite. The claims have been amended to provide more clarity, and the following paragraph uses language from the specification as filed to provide further clarification. No new matter has been added.

The functional random instruction test (FRIT) kernel is software “which generates one or more tests in real time when loaded on-board a complex device such as a microprocessor under test,” See page 10, lines 7-11, also denoted as [pg. 10; lns. 7-11]. “When loaded on-board a complex device such as a microprocessor under test ..., the FRIT kernel ... will activate the complex device under test ... to generate and execute its own functional test sequences in real time.” [pg. 10; lns. 11-13]. The FRIT kernel is “converted into a test format (i.e., kernel test patterns)” before being loaded into memory in a tester. [pg. 13; lns. 4-5]. The “kernel test patterns,” therefore, correspond to a FRIT kernel that has been converted to a “test format” that is understandable to a tester. The tester “load[s] the kernel test patterns ... into on-board memory ... of the complex device under test” and “enable[s] execution of the kernel test patterns.” [pg. 13; lns. 12-15]. This corresponds to loading the FRIT kernel on board a device under test and activating the device under test to generate and execute its own functional test. See the first and second quoted passages in this paragraph.

By way of restating a portion of the previous paragraph, the term “kernel test patterns” refers to the FRIT kernel in a format understandable to a tester. The tester loads the kernel test patterns (which is a converted version of the FRIT kernel) to the device under test in the same

manner that the tester would load test patterns to any device under test. After the FRIT kernel is downloaded to the device under test, the FRIT kernel is activated to generate and perform tests.

Applicants respectfully submit that the clarification provided in the previous two paragraphs along with the clarifying language now in independent claims 1, 11, 21, and 31 show that the claims are not indefinite within the meaning of 35 USC § 112, second paragraph.

Accordingly, applicants respectfully request that the rejection be withdrawn.

§102 Rejection of the Claims

Claims 1-4, 6, 11-14, 16, 21-24, 26 and 31-34 were rejected under 35 USC § 102(b) as being anticipated by Williams et al. (U.S. 2002/0093356), referred to herein as the “Williams reference.” Applicants traverse this rejection.

Applicants respectfully submit that the Williams reference does not disclose, teach, or suggest the subject matter of independent claim 1 as amended, including for example, “executing software within the FRIT kernel on the complex device under test.” Accordingly, applicants respectfully believe that claim 1 is in condition for allowance. Claims 2-4 and 6 are also believed to be in condition for allowance at least by virtue of dependency on claim 1.

Applicants respectfully submit that the Williams reference does not disclose, teach, or suggest the subject matter of independent claim 11 as amended, including for example, “enabling execution of software within the FRIT kernel on the complex device under test.” Accordingly, applicants respectfully believe that claim 11 is in condition for allowance. Claims 12-14 and 16 are also believed to be in condition for allowance at least by virtue of dependency on claim 11.

Applicants respectfully submit that the Williams reference does not disclose, teach, or suggest the subject matter of independent claim 21 as amended, including for example, “enabling execution of software within the FRIT kernel on the complex device under test.” Accordingly, applicants respectfully believe that claim 21 is in condition for allowance. Claims 22-24 and 26 are also believed to be in condition for allowance at least by virtue of dependency on claim 21.

Applicants respectfully submit that the Williams reference does not disclose, teach, or suggest the subject matter of independent claim 31 as amended, including for example, “a processor to perform a ... test of the complex device under test (DUT) upon execution of the FRIT kernel.” Accordingly, applicants respectfully believe that claim 31 is in condition for

allowance. Claims 32-34 are also believed to be in condition for allowance at least by virtue of dependency on claim 31.

Regarding claims 2, 3, 12, 13, 22, 23, 32, and 33, the office action incorrectly equates the ATPG tool 12 of Williams with the FRIT kernel/SBE of the claimed invention. The ATPG tool of Williams is external to the device under test, whereas the FRIT kernel/SBE of the claimed invention is resident within the device under test when the test is run. Applicants respectfully submit that for these reasons, the claimed invention further defines over the references of record.

Regarding claims 4, 14, 24, and 34, the office action incorrectly equates the central processor 101 of Williams with the test program execution module of the claimed invention. The central processor 101 of Williams is a hardware processor that is part of an ATPG system. See paragraph 53 of the Williams reference. In contrast, the test program execution module of the claimed invention is part of a software kernel that executes on a device under test. Applicants respectfully submit that for these reasons, the claimed invention further defines over the references of record.

§103 Rejection of the Claims

Claims 7, 8, 17, 18, 27, 28 and 36 were rejected under 35 USC § 103(a) as being unpatentable over Williams et al. Applicants traverse this rejection. As an initial matter, applicants respectfully submit that this rejection, in order to support a *prima facie* case of obviousness, relies on the anticipation of the independent claims by the Williams reference. As described above, applicants respectfully submit that the Williams reference does not teach each and every claim limitation in the independent claims, and so the *prima facie* case of obviousness in this rejection necessarily fails. The above comments notwithstanding, additional arguments for withdrawal of the rejection under 35 USC § 103(a) are provided below.

Regarding claims 7, 17, 27, and 36, the claims have been amended to clarify that the device under test performs the actions listed “when software within the FRIT kernel is executed” by the device under test. Applicants respectfully submit that the Williams reference does not disclose, teach, or suggest the device under test executing software of a FRIT kernel. The Office action states that Williams suggests moving a linear feedback shift register (LFSR) to the device under test. Applicants respectfully submit that if one were to move the shift register of Williams

to a device under test, one would not arrive at the subject matter of claims 7, 17, 27, and 36. Further, the Office Action states that “it would have been obvious to one of ordinary skill in the art at the time the invention was made to move the test sequence generation and execution functions to the DUT.” Applicants respectfully disagree. Moving a shift register to a device under test does not in any way hint at loading a software kernel into a device under test. Applicants respectfully submit that the only way to arrive at this result when modifying the Williams reference is to use hindsight in light of applicants’ patent application, which is, of course, impermissible.

Claims 5, 9, 10, 15, 19, 20, 25, 29, 30, 35, 37 and 38 were rejected under 35 USC § 103(a) as being unpatentable over Williams et al. in view of Gittinger et al. (U.S. 5,668,815), hereinafter referred to as the “Gittinger reference.” Applicants traverse this rejection. Applicants respectfully submit that this rejection, in order to support a *prima facie* case of obviousness, relies on the anticipation of the independent claims by the Williams reference. As described above, applicants respectfully submit that the Williams reference does not teach each and every claim limitation in the independent claims, and so the *prima facie* case of obviousness in this rejection necessarily fails.

Reservation of Rights

Applicants do not admit that references cited under 35 USC §§ 102(a), 102(e), 103/102(a), or 103/102(e) are prior art, and reserve the right to swear behind them at a later date. Arguments presented to distinguish such references should not be construed as admissions that the references are prior art.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant’s attorney (952-473-8800) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-2359.

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 09/917661

Filing Date: July 31, 2001

Title: FUNCTIONAL RANDOM INSTRUCTION TESTING (FRIT) METHOD FOR COMPLEX DEVICES SUCH AS MICROPROCESSORS

Assignee: Intel Corporation

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Dkt: 80107.051US1 (INTEL)

Respectfully submitted,

PRAVEEN PARVATHALA ET AL.

By Their Representatives,
LeMoine Patent Services, PLLC
c/o PortfolioIP
P.O. Box 52050
Minneapolis, MN 55402
952-473-8800

Date 6-15-04

By Dana B. LeMoine
Dana LeMoine
Reg. No. 40,062

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 15 day of June, 2004.

Emily Bates
Name

Emily Bates
Signature